

REMARKS

In response to the Office Action dated February 14, 2006, Applicant respectfully requests reconsideration.

As a preliminary matter, in the response to arguments section, the Office Action appears to argue that the technical advantages are not reflected in the claims. Therefore, Applicant has amended independent claims 1 and 12. In particular, independent claim 1 has been amended to now recite error checking circuitry for performing error checks based on mathematical functions wherein the multiplexing circuitry is arranged to selectively connect an incoming data signal from the output stage and a zero signal to set data input nodes of the register and wherein said multiplexing circuitry comprises a multiplexor arranged to supply a common term signal to a plurality of said data input nodes.

Claim 12 has now been amended to recite a method of checking an incoming bit stream for errors, wherein said step of supplying said plurality of input signals is performed using multiplexing circuitry arranged to selectively connect an incoming data signal from the input stage and a zero signal to said data input nodes of the register, and wherein the multiplexing circuitry comprises a multiplexor arranged to supply a common term signal to a plurality of said data input nodes.

Accordingly, claim 1 clearly distinguishes over Higuchi and Erickson individually and in any combination.

Claims 5-11 depend from claim 1 and are allowable for at least the same reasons.

Claim 12 clearly distinguishes over Higuchi and Erickson individually or in any combination and is in allowable condition.

The present specification describes performing an error check such as a cyclic redundancy check (CRC) by shifting an incoming bit stream through a register comprising a plurality of delay elements such as flip flops, and then feeding back an output from a selected stage of the register to an input stage of the circuit. For example, in the embodiment of Figure 4, the output fb₃₁ is fed back to the input stage 450 where it is combined with the input 452 and applied to various stages 430, 431, etc. of the register via a multiplexor 470 or 472.

The multiplexing circuitry recited in the claims is now defined as comprising a multiplexor arranged to supply a common term signal to a plurality of the data input nodes of the register. There

is simply no teaching anywhere in Higuchi or Erickson of a multiplexor to supply a single output to a plurality of input nodes to the register. To the contrary, as can be seen from Figures 1 and 2 of Higuchi and Figure 6 of Erickson, each flip flop of the registers in these two references requires its own respective multiplexor. That is the multiplexors 13₁ to 13₇ in Figure 2 of Higuchi, and the multiplexors 88 in Figure 6 of Erickson.

Furthermore, one skilled in the art would not be motivated to combine Higuchi and Erickson as suggested in the Office Action. The Office Action has failed to make out a prima facie case of obviousness because the Office Action has failed to suggest any motivation as to why a person skilled in the art would combine Erickson with Higuchi. The Office Action states that "it would have been obvious to one of ordinary skill in the art at the time of the invention to use the multiplexing circuitry of Erickson in place of the multiplexing circuitry of Higuchi. This would have been obvious to one of ordinary skill in the art at the time of the invention to do this because the two circuits function the same by providing the same result for the same purpose". However, for exactly this reason, a person of ordinary skill in the art would not modify Higuchi to include the circuitry from Erickson. There is no motivation for a skilled person to modify the circuitry of Higuchi in order to provide exactly the same result and a skilled person would therefore have no reason to do so. The skilled person would not go out of their way to modify the circuitry of Higuchi if they believed it would produce exactly the same result.

In view of the fact that there is no motivation to combine Higuchi and Erickson and the fact that the claims distinguish over the references, either individually or in combination, Applicant believes that the application is now in allowable condition.

CONCLUSION

In view of the above amendment, the pending application is believed to be in condition for allowance.

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, any necessary extension of time is hereby requested. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Dated: May 15, 2006

Respectfully submitted,

Rogrigo CORDERO, Applicant

By 

James H. Morris

Registration No.: 34,681

WOLF, GREENFIELD & SACKS, P.C.

Federal Reserve Plaza

600 Atlantic Avenue

Boston, Massachusetts 02210-2206

(617) 646-8000